WHAT IS CLAIMED IS:

1. Circuitry for controlling the oscillating frequency of an oscillator, the circuitry comprising:

a plurality of capacitors, each of which is independently selectable by a control signal, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator.

2. The circuitry of claim 1, wherein each of the plurality of capacitors has a different capacitance than the other capacitors, and a predefined amount of capacitance is provided by a predetermined combination of capacitors.

3. The circuitry of claim 2, wherein the capacitors are drain-source connected MOSFETs.

4. The circuitry of claim 3, wherein the MOSFETs are P-type enhancement mode MOSFETs.

5. The circuitry of claim 3, wherein the MOSFETs are N-type depletion mode MOSFETs.

6. The circuitry of claim 1 wherein the capacitors are selected from the group consisting of on-chip metal capacitors, on-chip poly capacitors, and discrete capacitors.

7. The circuitry of claim 1, wherein each of the capacitors corresponds to a transmission gate switch.

8. The circuitry of claim 7, further comprising a set of memory registers to provide the control signals for selecting the individual capacitors

9. The circuitry of claim 8, wherein the transmission gate switches are decoupled from the set of memory registers by a set of buffer circuitry.

10. The circuitry of claim 9, wherein the set of buffer circuitry is powered by a filtered power signal.

11. The circuitry of claim 1, wherein the oscillator includes a resonator and an inverting amplifier.

12. The circuitry of claim 11, wherein a first subset of the plurality of capacitors is selectively electrically coupled to a first terminal of the resonator, and a second subset of the plurality of capacitors is selectively electrically coupled to a second terminal of the resonator

13 An electronic device comprising:

a real time clock for generating a system time signal, the real time clock having a digitally tunable oscillator for

digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal; and

a memory device for storing data representing a configuration of the digitally adjusted tunable oscillator.

14. The electronic device of claim 13, further comprising a communication port for receiving a reference time signal, wherein the digitally tunable oscillator is digitally adjusted according to the reference time signal to minimize the difference between the system time signal and the reference time signal.

15. The electronic device of claim 13, wherein the digitally tunable oscillator includes a capacitor bank having a set of capacitors with capacitance values in a binary-weighted relationship, the capacitors selectable through a set of control signals.

16. A method comprising:

generating a set of control signals to select a subset of capacitors from a set of capacitors;

connecting the selected subset of capacitors to an oscillator;

generating an oscillating signal using the oscillator and the selected subset of capacitors in combination; and

generating a system time signal using the oscillating signal.

17. The method of claim 16, further comprising receiving a reference time signal, comparing the reference time signal with the system time signal, and modifying the set of control signals in response to the difference between the reference time signal and the system time signal to select a different subset of capacitors.

18. The method of claim 17, further comprising saving data representing the setting of the control signals in a memory.

19. A method of generating a time signal comprising:

generating a system time signal using a real time clock circuit that has a tunable oscillator for adjusting an operation frequency of the real time clock circuit;

receiving a reference time signal over a network;

adjusting the tunable oscillator to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal.

20. The method of claim 19 wherein adjusting the tunable oscillator comprises adjusting a set of control signals to

modify a selection of a set of capacitors within a capacitor bank, the selection of the set of capacitors correlating to the operating frequency of the real time clock circuit.

21. Apparatus for providing a variable level of capacitance, comprising:

a plurality of capacitors, each capacitor selectable through an independent control signal generated by a logic circuit, the selected capacitors providing an amount of capacitance that is the sum of the individual capacitances of the selected capacitors; and

buffer circuitry for decoupling the plurality of capacitors from the logic circuit to prevent noise in the logic circuit from affecting the plurality of capacitors.

22. The apparatus of claim 21, further comprising a filter circuit connected to a power supply to generate a filtered power supply signal that is used to power the buffer circuitry.

23. The circuit of claim 21, further comprising transmission gates, each of which corresponds to one of the plurality of capacitors and can be turned on by the independent control signal when the corresponding capacitor is selected.

24. Apparatus comprising:

a control unit configured to generate a set of control signals, each of which independently selects a capacitor from a plurality of capacitors, the selected capacitors being coupled to an oscillator, the selected capacitors in combination proving a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator.

25. The apparatus of claim 24 in which the control unit is disposed within a computer chipset.

26. The apparatus of claim 24, further comprising circuitry for generating a system time signal based on the oscillating frequency of the oscillator.

27. The apparatus of claim 26, further comprising a memory for storing the configuration of the set of control signals, and a data processing unit that processes data based on the system time signal.